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Real Time SOC Based Low Cost Smart Sensor Using DWT on FPGA

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ABSTRACT: In this world of fast growing technology all the monitoring systems require the features like high performance instrumentation, low-cost primary sensors, online signal processing, portability, and versatility. Introduction of smart sensor comes up with all these features. Commercially available monitoring equipment cannot easily achieve versatility and portability. But smart sensor approach will increase the performance and overcome costs in monitoring systems. They use standard off-the-shelf sensors and add signal processing, communication and integration capabilities in their functionality. This paper proposes implementation of real time system-on-chip (SOC) based smart sensor for time-frequency analysis of the signals like voltage, electric current and vibrations by applying discrete wavelet transform (DWT) on field programmable gate array(FPGA). The proposed smart sensor uses a proprietary hardware processing unit. This unit includes a multiplier accumulate unit (MAC) for computing real time discrete wavelet transform for all the input signals. The proposed designs of MAC uses a modified booth multiplier and carry save adder for area optimization and propagation delay. This design can connect to different primary sensors without additional instrumentation and shows obtained results in 2-D view on a video graphics array screen or liquid crystal display. For presentation purposes, hardware computed results will be sending to a PC through an RS232 interface and plotting in MATLAB. The SOC-based smart sensor module will be designing and developing in Xilinx 12.2 ISE using VHDL and simulating in Modelsim 6.3f.

KEYWORDS: smartsensor; discrete wavelet transform; area optimization; propagation delay

I. INTRODUCTION

Today's monitoring systems require demanding tasks like high performance instrumentation, low cost primary sensors, and characteristics of online signal processing [1-3]. Portability and versatility are not easily met by commercially available monitoring equipment. But the utilization of smart sensors is an approach to increase performance and overcome costs in monitoring systems. They use standard off-the-shelf sensor and add signal processing, communication and integration capabilities in their functionality [4,5]. This paper is a smart sensor, integrated as a low-cost SOC. The proposed smart sensor is based on a reconfigurable hardware processing unit implemented into FPGA. It can connect to different primary sensors to increase performance capabilities that allow the smart sensor to apply wavelet transform (WT) analysis on the acquired signal, with different parameters like mother wavelet and decomposition level. Obtained results can be presented to the user in a 2-D view.The proposed smart sensor permits modification or redefinition of the implemented algorithm without changing the hardware itself. It extracts relevant time-frequency information from different sampled signals such as voltage, electric current, and vibrations, among others, to carry out complete system monitoring [6].

II. THEORETICAL BACKGROUND

A. Wavelet Transform (WT) WT is used for extracting time-frequency information from time-dependent signals [7,8]. It is capable to give frequency decomposition of a signal through time by isolating its frequency evolution. Continuous WT is defined through the wavelet coefficients (WC) produced by the convolution of a signal x(t) with a mother wavelet function $\psi(t)$ [9,10]. The transformationprocess gives a timescale decomposition of the original signal. The concept of scale is related to the concept of frequency and corresponds to a timescale a of function $\psi(t)$. DWT has shown its value in analyzing non stationary signals [7 , 8]. It is computed using a set of discrete-time lowand high-pass filters h(i, j) and g(i, j), respectively, followed by a signal down sampling operation for each decomposition level; this method is known as Mallat algorithm. Indices i and j represent decomposition level and transformation-node number, respectively, as depicted in Fig. 1. According to this algorithm, the original discrete signal x(n) is decomposed into its low-and high-frequency components named approximation (ACi) and detail (DCi), respectively, at level i. Decomposition is successively applied to AC in order to obtain subsequent low- and high-frequency bands down to the desired level L. Signal reconstruction is done by applying the decomposition process in an inverse way. This time, each reconstruction level s followed by a signal up sampling operation. This is known as the inverse DWT (IDWT).

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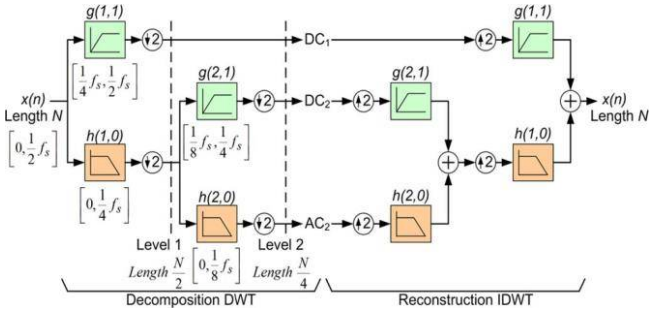

Figure 1. Mallat algorithm for wavelet decomposition and reconstruction of discrete signals

III. SMART SENSOR IMPLEMENTATION

A smart sensor provides signal processing and communication capabilities to the primary sensor [11]. Characteristics uch as portability and integration are included by implementing the smart sensor as a SOC. *Fig. 2* depicts the block diagram of the proposed smart sensor realized into an FPGA-based SOC. All its components are developed in a very high-speed integrated circuit hardware description language (VHDL) as proprietary cores. During time-frequency analysis for system monitoring, the signal is acquired and conditioned in the data acquisition system (DAS). A hardware processing unit is used for real time computation of DWT. Memory is required for temporal storage of information, and interfaces such as liquid crystal display (LCD), video graphics array (VGA), USB, and RS232 are used for displaying results to users or transferring information to a PC. The interfaces for information transference can be easily incorporated into the smart sensor by developing the hardware description of their corresponding drivers. A new architecture of the SOC based smart sensor has been designed, that is better than the previous architectures since the hardware required to implement it is reduced. Real time computation of DWT is based on MAC unit. In this proposed design of MAC unit the basic multiplier and adder circuits are replaced by a booth multiplier and carry save adder for increasing speed with minimum power and less propagation delay.

A. DATA ACQUISITION SYSTEM(DAS)

Data acquisition is the process of sampling signals that measure real world physical conditions and converting the resulting samples into digital numeric values that can be manipulated by a computer [12]. Data acquisition system typically converts analog waveforms to digital values. The ADC0808 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter,8channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

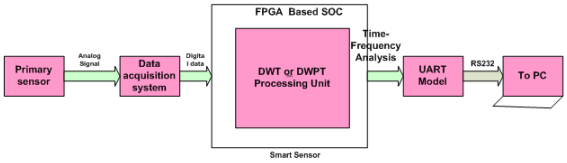

Figure 2. Block Diagram of the proposed smart sensor

The device eliminates the need for external zero and fullscale adjustments. Easy interfacing to microprocessors isprovided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE outputs. The design of the ADC0808 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power [13]. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications.

B. DWT HARDWARE PROCESSING UNIT

DWT implementation is particular cases of the finite-impulse-re sponse filter with M th order filter coefficients. The FIR filter is designed by using low cost and high speed MAC unit. Depending on the applied analysis, the DWT hardware processing unit may require a decomposition DWT module or decomposition and reconstruction IDWT modules. This can be defined by the user along with the desired decomposition levels and the applied mother wavelet function during the smart sensor configuration.

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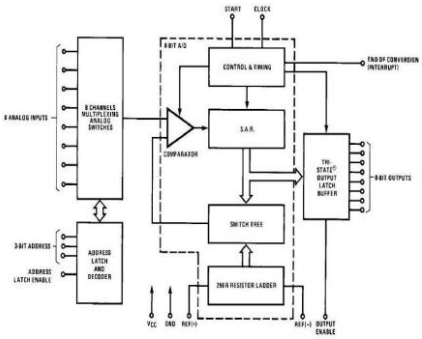

Figure 3. Block diagram of data acquisition system-ADC0808

C. DECOMPOSITION DWT

During decomposition, the corresponding DWT coefficients is extracted from a ROM device and multiplied by the current signal sample x (n); when a new sample is acquired, this operation is repeated and partial results are accumulated. If reconstruction is required, partial decomposition coefficients are stored into on-chip block-RAM modules; otherwise, the proposed smart sensor can be configured to provide these coefficients at its output. The block diagram of the DWT decomposition is depicted in *Fig.4*

D. RECONSTRUCTION IDWT

Signal reconstruction IDWT is carried out by multiplying DWT or DWPT coefficients by the corresponding wavelet components stored in on-chip block-RAM, which were obtained during signal decomposition. This procedure obtains a reconstructed sample x_(n), as depicted in Fig. 5.

E. UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER(UART)

UART is a device that has the capability to both receive and transmit serial data. UART exchanges text data in an American Standard Code for Information Interchange (ASCII) format in which each alphabetical character is encoded by 7 bits and transmitted as 8 data bits. For transmission the UART protocol wraps this 8 bit sub word with a start bit in the least significant bit (LSB) and a stop bit in the most significant bit (MSB) resulting in a 10 bit word format. This includes Baud rate generator, transmitter and receiver.

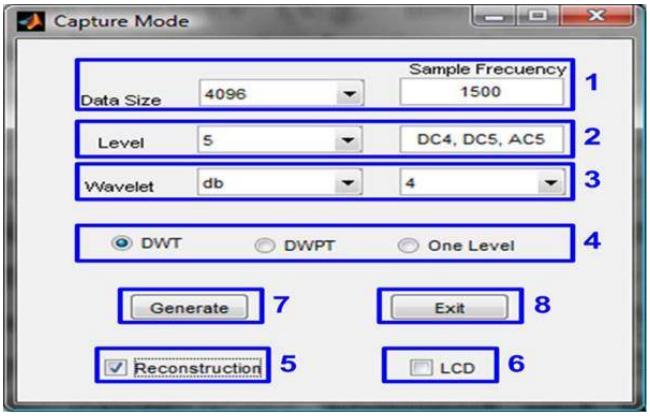

Figure 8 . GUI tool for hardware and software generation during the smart

sensor implementation This application generates VHDL and assembly language code corresponding to the hardware in the smart sensor implementation and the program executed by the embedded microprocessor. Through this GUI tool shown in *Fig.5*, the user does not have to write any code for reconfiguring the smart sensor. During the smart sensor configuration, the user has to define parameters.

IV. RESULTS

Fig.10-14 shows the results obtained after functional verification of the DAS DWT processing unit with modified MAC unit which includes booth multiplier and carry save adder and UART interface. These modules are is designed in VHDL and simulated on Xilinx 12.2 ISE. The expected outcome would show reduction in area and increase in speed of the proposed design.

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Figure 10. The simulation waveform of Data Acquisition System

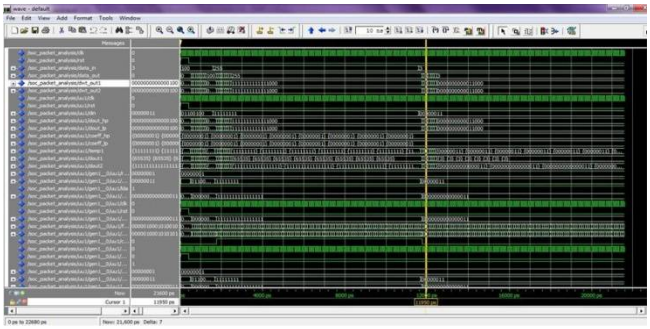

Figure 11. Simulation result of DWT hardware processing Unit with modified MAC

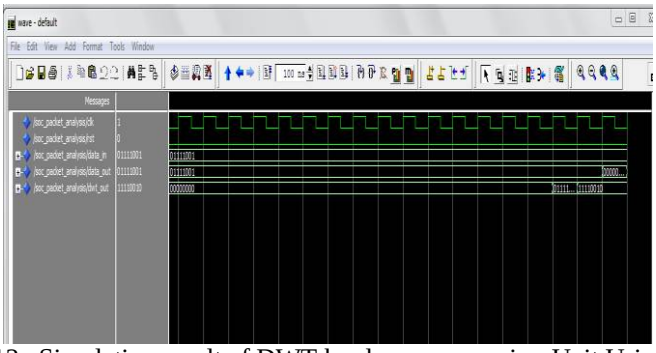

Figure 12. Simulation result of DWT hardware processing Unit Using MAC

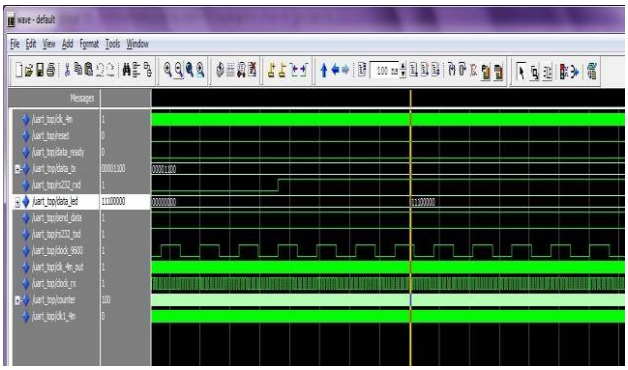

Figure 13. The simulation waveform of UART interface

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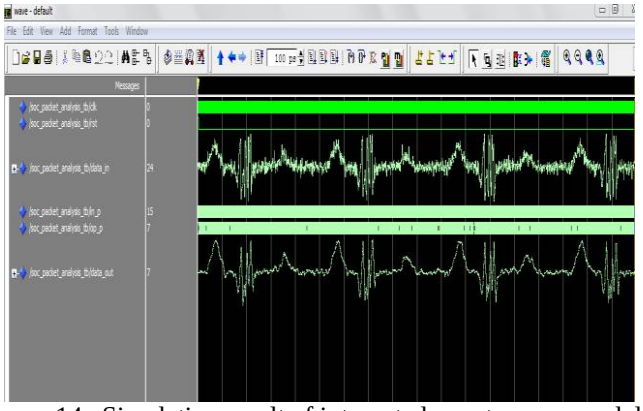

Figure 14. Simulation result of integrated smart sensor module

Table 2 and 3 shows the device utilization summary obtained from the synthesis report of structural modeling of hardware processing unit with modified MAC unit and without MAC unit using Haar transform in DWT. Byanalyzing the synthesis results there is less number of look up tables and slice filp flops are required for modified MAC unit compared to conventional MAC unit.

Table 2: Device utilization summary of hardware processing unit with modified MAC unit

Logic Utilization	Used	Available	Utilization
Number of slices	540	3584	15%
Number of slice flip flops	64	7168	0%
Number of 4 input LUTs	734	7168	10%
Number of bonded IOBs	18	141	12%
Number of GCLKs	1	8	12%

Table 3: Device utilization summary of hardware processing unit without MAC

Logic Utilization	Used	Available	Utilization
Number of slices	1619	3584	45%
Number of slice flip flops	2432	7168	33%
Number of 4 input LUTs	1495	7168	20%
Number of bonded IOBs	18	141	12%
Number of GCLKs	1	8	12%

The delay and frequency of hardware processing unit with modified MAC unit and the delay and frequency of hardware processing unit without MAC by using haar transform in DWT is as shown in Table 4. This shows there is reduction in delay of the proposed smart sensor with modified MAC when compared to the other design. Table 4: Timing Summary of DWT hardware processing unit DWT hardware processing unit Delay Frequency Existing MAC 19.26ns 519.211 MHz Proposed MAC 12.229ns 81.771 MHz

V. CONCLUSION

The proposed smart sensor implementation is based on a low-cost FPGA device that adds characteristics of real-time processing, portability, and versatility, making it a helpful SOC solution for many applications. The proposed smart sensor features allow connecting it to other monitoring systems or a PC through different interfaces without additional instrumentation or equipment. The proposed smart sensor using modified MAC unit has less propagation delay and area. The results has compared with the previous smart sensor implementations to prove our motivation. The simulation

results established that the proposed low cost and high performance MAC unit based smart sensor improved speed and better monitoring features compared with the earlier reports.

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